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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte INTEL CORPORATION

Appeal 2007-4533
Application 10/659,133
Technology Center 2100

Decided: February 07, 2008

Before JAMESON LEE, RICHARD TORCZON, and SALLY C.
MEDLEY, *Administrative Patent Judges*.

TORCZON, *Administrative Patent Judge*.

DECISION ON APPEAL

The claims on appeal broadly pertain to the control of access to a resource by two or more components, particularly to selectively partitioning a resource, such as a cache, between components sharing the resource.¹ Claims 2-11, 13, 18, and 20 are pending. All have been rejected under

¹ Specification (Spec.) at 2:2-4.

35 U.S.C. § 103 for having been obvious. The appellant (Intel) seeks review of the rejection. We AFFIRM.

THE CLAIMS

Intel does not offer separate arguments for the claims. The claims thus stand or fall together. We select claim 11 as representative of the claims on appeal.² Claim 11 defines the invention as follows:

11. A method comprising:
controlling, with an access controller coupled to at least first and second components, which of said at least first and second components are able to access which elements of a selectively partitioned resource; and
storing in a register of said access controller a first mask value, wherein access to the partitioned elements is controlled based on said first mask value.

We must construe a claim as broadly as is reasonable in view of the specification, but may focus on the contested limitation.³ Intel points to the

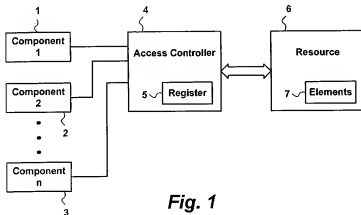


Fig. 1

requirement that access be controlled based on the first mask value.⁴ Intel discloses⁵ a block diagram showing an embodiment (FIG. 1, left) with a register 5 in

an access controller 4, and elements 7 of a resource 6. Claim 11 is, of

² 37 C.F.R. § 41.37(c)(1)(vii).

³ *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1256 (Fed. Cir. 2007).

⁴ Appeal Brief (Br.) at 4. Intel uses claim 2 to illustrate the limitation, but the limitation is common to both claims 2 and 11.

⁵ Spec. at 5-6.

course, not limited to this example, but we construe the claim broadly to be consistent with such an embodiment.⁶

Intel has not pointed us to a specific definition of "mask value" so we construe the phrase broadly, consistent with the function it performs in claim 11, as a string encoding information affecting access to the resource elements. Similarly, Intel has not argued for a specific definition of "controlled", so we construe the term broadly to mean access is affected by the mask value. The claim does not mandate any particular mode of control as long as the control is "based" on the mask value. We note that the claim uses "comprising" in transit from the preamble to the body of the claim, which means that the claimed method is open to the inclusion of other steps, including other steps that might also control access to the resource elements.

OBVIOUSNESS

The claims have been rejected as including subject matter that would have been obvious to a person having ordinary skill in the art in view of two United States patents to Ebrahim⁷ and Arimilli,⁸ respectively.⁹ The examiner relied on Arimilli to address the partitioning limitation.¹⁰ Since Intel has not disputed the obviousness of partitioning a cache resource, we focus our analysis on the Ebrahim patent.

⁶ *Primos, Inc. v. Hunter's Specialties, Inc.*, 451 F.3d 841, 848 (Fed. Cir. 2006).

⁷ Z. Ebrahim, K. Normoyle, S. Nishtala, & W.C. Van Loo, *Fast, dual ported cache controller for data processors in a packet switched cache coherent multiprocessor system*, US 5,644,753 (issued 1 July 1997).

⁸ R.K. Arimilli, J.S. Dodson, J.D. Lewis & T.M. Skergan, *Method for high-speed recoverable directory access*, US 5,867,511 (issued 2 February 1999).

⁹ Supplemental Examiner's Answer (Ans.) at 4.

¹⁰ Ans. at 4.

In analyzing obviousness, the scope and content of the prior art must be determined, the differences between the prior art and the claims ascertained, and the ordinary level of skill in the art resolved. Objective evidence of the circumstances surrounding the origin of the claimed subject matter (so-called secondary considerations) may also be relevant. One function of secondary considerations is to guard against the employment of impermissible hindsight.¹¹

¹¹ *Graham v. John Deere Co.*, 383 U.S. 1, 17, 36 (1966), *cited with approval in KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1732 (2007). The record on appeal does not contain objective evidence of secondary considerations.

Scope and content of the prior

The Ebrahim patent relates generally to systems in which processors share memory resources, particularly systems that minimize cache interference using cache controllers for each processor.¹² Ebrahim provides a block diagram (FIG. 1, right) showing an embodiment of the system. The system has components (UPA Modules_{1-n},

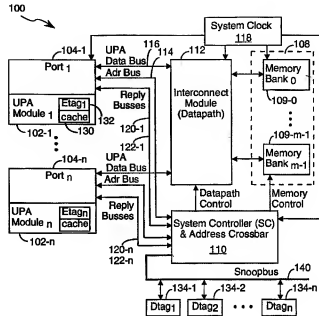


FIGURE 1

102-1-102-n), a system controller (SC, **110**), and a resource **108** with elements (Memory Banks 0 - m-1, **109-0 – 109-m-1**). The system controller **110** has a number of registers, including a SC ID register **180**, which includes a 5-bit mask field (UPANUM, **182**). Ebrahim teaches that the UPANUM "specifies the maximum number of UPA ports the System Controller can support."¹³ The examiner found that the UPANUM is used to manage UPA port **104-1-104-n** requests **P_REQ**.¹⁴

Differences between the prior art and the claims

¹² Ebrahim at 1:8-16.

¹³ Ebrahim at 21:58-22:10; Fig. 5.

¹⁴ Ans. at 11-13, citing Ebrahim at 7:13-8:4 and 11:46-12:4.

The examiner cites partitioning as a difference, which the Arimilli patent is said to resolve for the purposes of obviousness. Intel provides no argument to the contrary.

Intel urges that Ebrahim does not teach a mask value in an access-controller register used to control access to the partitioned elements. Intel argues that the purpose of the UPANUM mask is unclear, but in any case it does not control access to resource elements.¹⁵

The ordinary level of skill

We look to the evidence of record—the applicant's disclosure, the cited references, and any declaration testimony—in resolving the ordinary level of skill in the art. We focus on what those of skill in the art know and can do.¹⁶

According to Intel's specification, the desirability of a cache memory resource to speed memory operations was known in the art.¹⁷ Several algorithms were known for managing the cache.¹⁸ A person having ordinary skill in the art would appreciate that cache memory can be organized with a number of blocks or ways.¹⁹ Such a person had the skill to implement a method in hardware and software based on a high-level description.²⁰

According to Ebrahim, the art well knew the importance of managing a shared cache memory to avoid conflicts that arise when more than one

¹⁵ Br. at 5.

¹⁶ *Ex parte Jud*, 85 USPQ2d 1280, 1282 (BPAI 2007) (rehearing with expanded panel).

¹⁷ Spec. at 2.

¹⁸ Spec. at 3-4.

¹⁹ Spec. at 6-7.

²⁰ Spec. at 18-20.

component is using shared address space in the cache.²¹ Ebrahim notes that there are a number of approaches to maintaining cache coherence, including the use of a system controller to control access to the cache.

ANALYSIS

The examiner and Intel appear to have different understandings of the scope of the claims. In particular, the examiner understands "access to the partitioned elements is controlled based on said first mask value" very broadly to include any effect on access as a result of the mask value. With this understanding in mind, the examiner has explained that the UPANUM mask affects how the system controller interacts with the components, which indirectly affects access to the cache elements. Indeed, the examiner notes that in the extreme case where the UPANUM mask is set to zero, none of the components will have access to any of the cache elements.²² In effect, the UPANUM indirectly controls access up to and including the state of no access at all.

While the examiner's construction is very broad, the literal language of claim 11 is also extraordinarily broad. We cannot say that the examiner's construction is unreasonable. While the specification contains a wealth of detail on how the invention could be implemented, it also contains a high-level discussion of the invention without that detail. Claim 11 itself is strikingly devoid of detail on how access control is achieved other than that it involves a mask value in an access-controller register. Thus, the literal language of the claim permits indirect control as do the broadest descriptions of the invention. The obligation to draft a claim covering the invention lies

²¹ Ebrahim at 1:19-25.

²² Ans. at 11-13.

with the applicant.²³ In this case, claim 11 is much broader than what the applicant appears to have actually invented and, as a consequence, it covers subject matter already obvious in the prior art.

CONCLUSION

Intel has not demonstrated prejudicial error in the rejection of claim 11 when it is construed as broadly as is reasonable in view of the specification. Since the claims stand or fall together, the rejection of all pending claims under § 103 is—

AFFIRMED

MAT

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²³ *In re Morris*, 127 F.3d 1048, 1057 (Fed. Cir. 1997).